**EECE 2323 Digital Logic Design Lab Report**

Lab 1 and Title

| Student Name: Ousmane Toure | Section #: |
| --- | --- |
| Instructor Name: Dr. Abolela  Lab TA Name: | Date: |

1. **Background & Purpose**: The background should be only one paragraph that contains the goals of the lab and briefly explains what significance it has to the scientific community.

State the objective of the lab exercise. Though this is provided in the lab documents, the purpose should be restated in your own words. The purpose should be specific and focus on scientific principles. *Example*: In this lab, the Xilinx Vivado software was introduced and used to design an XOR function using NAND gates.

In a sentence or two, explain why the purpose of the lab is important to the scientific community. What is the motivation behind performing this lab? *Example*: Vivado software is one of the main software packages used in the design of logic circuits, and this lab shows the students how to use it to design simple logic circuits.

1. **Pre-Lab Response:** Include pre-lab responses in this section. These include, Verilog code, test- benches, simulation outputs, responses to any questions asked, etc. Each item should be labeled.

| a | b | f | ovf |
| --- | --- | --- | --- |
| 8’d0  00000000 | 8’d0  00000000 | 8’d0  0000000 | 0 |
| 8’d12  00001100 | 8’d34  00100010 | 8’d46  00101110 | 0 |
| -8’d12  11110100 | -8’d34  11011110 | -8’d46  11010010 | 0 |
| 8’d100  01100100 | -8’d50  11001110 | 8’d50  00110010 | 0 |
| -8’d100  10011100 | 8’d50  00110010 | -8’d50  11001110 | 0 |
| 8’d100  01100100 | 8’d100  01100100 | -8’d56  11001000 | 1 |
| -8’d100  10011100 | -8’d100  10011100 | 8’d56  00111000 | 1 |
| -8’d13  11110011 | 8’d12  00001100 | -8’d1  11111111 | 0 |
| -8d13  11110011 | -8d13  11110011 | -8’d26  11100110 | 0 |

2. Write a Boolean or verilog equation for the overflow output ovf based on input values a and

a[7] b[7] f[7]

A’B’F+ABF’

A[7]B[7]^F[7] + A[7]’B[7]’^F[7]

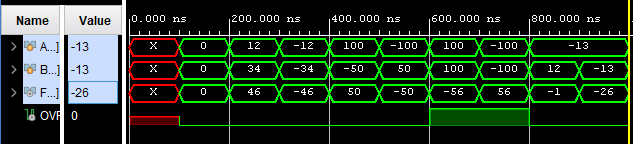
3. A good simulation testbench tests that every input and output bit can take the values zero and one. For the values in question 1 answer the following questions:

(a) The adder has 16 bits of input and 9 bits of output. Do the values in question 1 taken together set every input bit to both one and zero and every output bit to both one and zero? Explain your answer. Identify which bits are not tested in this manner.

No, because the [0] bit is not tested as there is no negative numbers. this means that they are always 0 and never checked for 1

(b) Add additional input ( a and b) values that test every bit in both the inputs and outputs so that every bit takes either a zero or a one value in your test cases.

highlighted in table



1. **Summary of Design Implementation**
   1. **Results and Analysis:** In only one paragraph, summarize the most important results and trends in the experiment. Figures, tables, or code in the pre-lab section or in an appendix can be referenced to support your analysis.

* State results and content independent of your own influence. These observations should be relevant to the purpose of the lab experiment.
* Describe trends and implications by referencing your results. What can you infer from your data/output? *Example*: Decreasing the gate delay shortens the propagation delays on the output, as shown in Figure 4. An overflow was observed when values were out of range.
* Briefly describe possible errors and discuss potential solutions.
  1. **Conclusion & Recommendations:** The final paragraph should emphasize the conclusions drawn from the results and how the results can be used in your scenario.
* State your conclusions based on the results of the lab.
* Provide recommendations for the scenario posed at the beginning of the lab procedure, based on the lab results. *Example*: Based on the results of the procedure, it is recommended to use at least 10 test values to exhaustively verify correct behavior of the design.

1. **Appendices**: Create a new appendix for each category of content ***not included in the pre-lab section****.* Title each appendix using the format *Appendix A: Descriptive Title*. For example, the summary report might contain the appendices:

* Appendix A: Design Program Files (Verilog modules, testbenches, etc)
* Appendix B: Captures of the output screens and simulation waveforms.

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